PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/13/7707
Dated 19 Mar 2013

M24LR04E-R, M24LR16E-R, M24LR64E-R Dual Interface

EEPROM Refined design

Table 1. Change Implementation Schedule

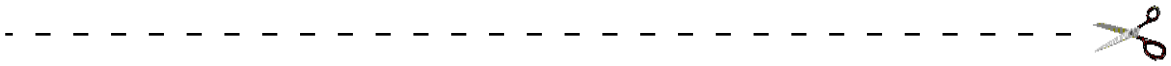
Forecasted implementation date for change	12-Mar-2013
Forecasted availability date of samples for customer	12-Mar-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	12-Mar-2013
Estimated date of changed product first shipment	18-Jun-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M24LR04E-R, M24LR16E-R, M24LR64E-R
Type of change	Product design change
Reason for change	Redesign refined for device limitations fix
Description of the change	Redesign refined
Change Product Identification	See marking paragraph
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/13/7707**
Please sign and return to STMicroelectronics Sales Office	**Dated 19 Mar 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Fidelis, Sylvain	Marketing Manager
Rodrigues, Benoit	Product Manager
Malbranche, Jean-Luc	Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

M24LR04E-R, M24LR16E-R, M24LR64E-R Dual Interface EEPROM Refined design

What is the change?

Following **devices limitations** described in the last revision of the corresponding **Errata sheet** (**rev. 2** in APPENDIX D), the **M24LR04E-R, M24LR16E-R and M24LR64E-R,** *4-Kbit, 16-Kbit and 64-Kbit Dual Interface EEPROM with password protection, energy harvesting and RF status protections family products*, has undergo through a **refined design** in order to fix:

- The RF field drop during I²C write cycle execution
- The SetRstEHEn command not functional in Addressed mode

As a consequence,

- Icc1 value has been changed from 40 µA to 100 µA at 5.5 V
- Icc1 at 1.8 V and 2.5 V being unchanged.

In addition, a T_Prog_flag bit has been added in the system memory to inform the application of proper execution of the write operation.

Datasheets of M24LR04E-R, M24LR16E-R and M24LR64E-R will be updated accordingly from current revisions respectively rev. 5, rev. 8, rev. 3 to new revisions respectively rev. 7, rev. 10, rev. 5.

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24LR04E-R, M24LR16E-R and M24LR64E-R with the refined design will improve service to our customers.

When?

The production of the M24LR04E-R, M24LR16E-R and M24LR64E-R with the design fix will ramp up from middle of March 2013 and shipments can start from end of June 2013 onward.

How was the change qualified?

The M24LR04E-R, M24LR16E-R and M24LR64E-R with the design fix have been qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

The **Qualification Reports** QRMMY1127, QRMMY1016, QRMMY1128 are available and included inside this document.

What is the impact of the change?

- Form: Marking change (see **Device marking** paragraph)

- Fit: No change

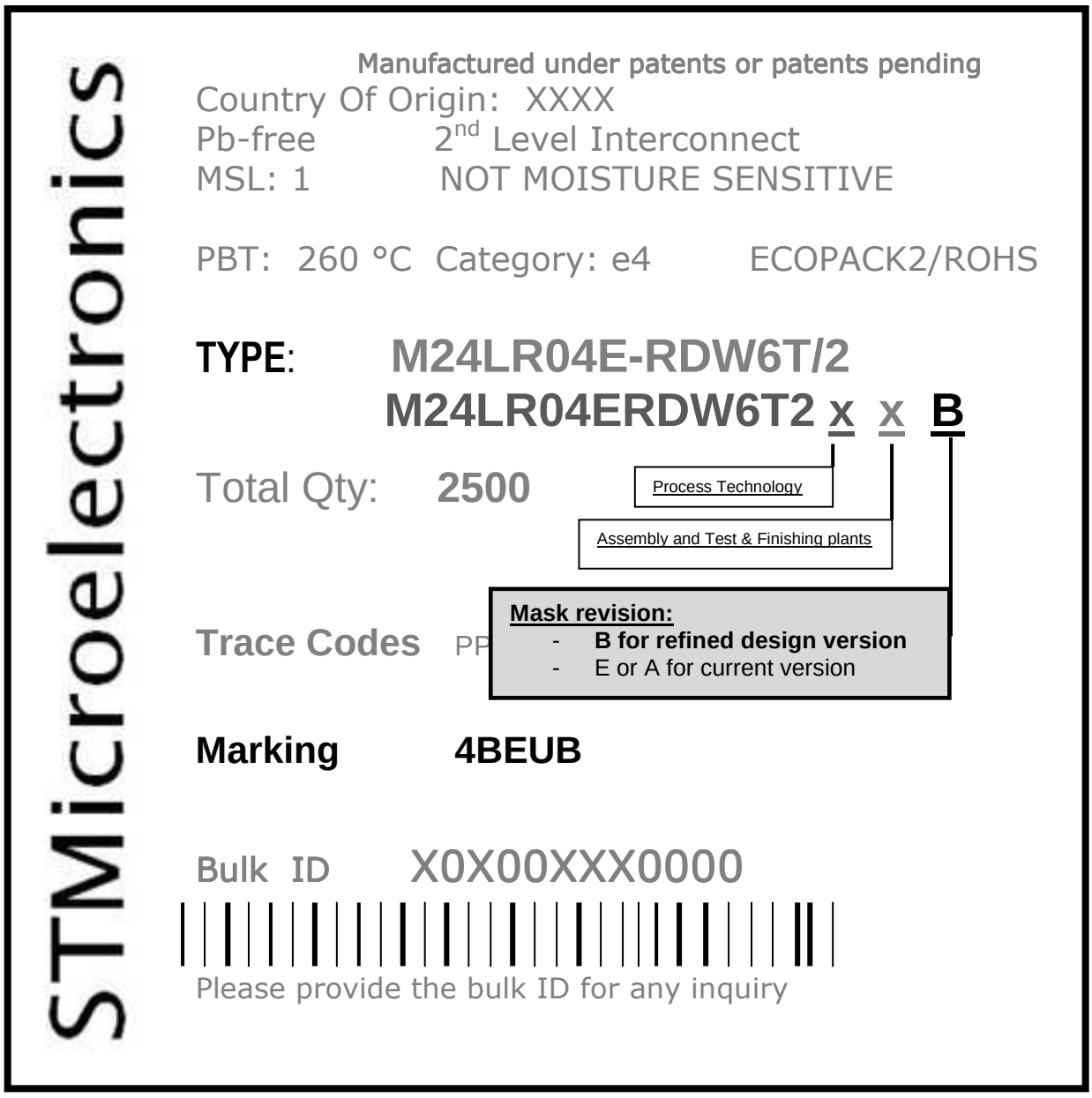
- Function: Change on DC characteristics Icc1 standby supply current and addition T_Prog_Flag bit in system area

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **Mask revision** identifier is "**B**" for the **refined design version**, this identifier being "E" (M24LR04E-R & M24LR16E-R) or "A" (M24LR64E-R) for the current version.

➔ *Example for M24LR04E-RDW6T/2*



How can the change be seen?

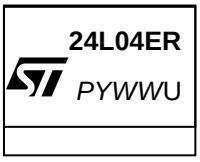
- DEVICE MARKING

For the device marking, the difference is visible inside the **product name** as following:

SO8N
Example:
M24LR04E-RMN6T/2
(See annex B for other products)

Refined design version

Current version



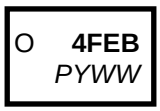
TSSOP8
Example:
M24LR16E-RDW6T/2
(See annex B for other products)

Refined design version

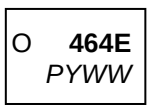
Current version

UFDFPN8
Example:
M24LR64E-RMC6T/2
(See annex B for other products)

Refined design version



Current version



P = Assembly plant / country
Y = Last digit of the Year of Assembly
WW = Assembly Week code
T = Process technology code/ Wafer Fab ID = U for current products

- IC REVISION IDENTIFICATION

All involved devices have the product revision set to 0xE and below (most significant nibble of 0x911 byte).

Appendix A- Product Change Information

Product family / Commercial products:	M24LR04E-R, M24LR16E-R and M24LR64E-R products family
Customer(s):	All
Type of change:	Product design change
Reason for the change:	Redesign refined for device limitations fix
Description of the change:	Redesign refined
Forecast date of the change: (Notification to customer)	Week 11 / 2013
Forecast date of Qualification samples availability for customer(s):	- Available for SO8N, TSSOP8 and UFDFPN8 - Bare die Week 14
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	**The Qualification Reports QRMMY1127, QRMMY1016, QRMMY1128 are available and included inside this document.**
Marking to identify the changed product:	See Device Marking paragraph
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 25 / 2013

Appendix B: Concerned Commercial Part Numbers:

Commercial Part Numbers	Package	Samples availability	Marking (*)
M24LR04E-RMN6T/2	SO8N	Available	**24LBERB** *PYWW***U**
M24LR04E-RDW6T/2	TSSOP8	Available	**4BEUB** *PYWW*
M24LR04E-RMC6T/2	UFDFPN8	Available	**4BEB** *PYWW*
M24LR04E-RUW20/2	BARE DIE	Week 14	N/A
M24LR16E-RMN6T/2	SO8N	Available	**24LDERB** *PYWW***U**
M24LR16E-RDW6T/2	TSSOP8	Available	**4DEUB** *PYWW*
M24LR16E-RMC6T/2	UFDFPN8	Available	**4DEB** *PYWW*
M24LR64E-RMN6T/2	SO8N	Available	**24LFERB** *PYWW***U**
M24LR64E-RDW6T/2	TSSOP8	Available	**4FEUB** *PYWW*
M24LR64E-RMC6T/2	UFDFPN8	Available	**4FEB** *PYWW*

*(*) Marking available also on **Datasheet** and **Errata sheet***

Appendix C: Qualification Report:

See following pages

QRMMY1128
Qualification report

New product / M24LR64E-R
using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24LR64E-RMN6T/2 M24LR64E-RDW6T/2 M24LR64E-RMC6T/2
Product description	64-Kbit EEPROM with password protection, dual interface & energy harvesting: 400 kHz I^2C bus & ISO 15693 RF protocol at 13.56 MHz
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore

Table 2. Package description

Package description	Qualified assembly plant location	Qualified final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product M24LR64E-R using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The voltage and the external RF carrier frequency covered by this document are:

- I^2C interface:
  - Single supply voltage: 1.8 to 5.5 V
- Contactless interface:
  - ISO 15693 and ISO 18000-3 mode 1 compatible
  - RF carrier frequency: 13.56 MHz ± 7 kHz

The temperature range covered by this document is:

- –40 to 85 °C

The CMOSF8H is a new advanced silicon process technology that has already been qualified in the ST Rousset 8” fab, and is in production for EEPROM products and also for dual interface EEPROM M24LR64/M24LR16E/M24LR04E products. This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

1.2 Conclusion

The new product M24LR64E-R using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

The M24LR64E-R device is a dual-interface, electrically erasable programmable memory (EEPROM). It features an I^2C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR64E-R is organized as 8192 × 8 bits in the I^2C mode and as 2048 × 32 bits in the RF mode.

The M24LR64E-R also features an energy harvesting analog output, as well as a user configurable digital output pin toggling during either RF write in progress or RF busy mode.

I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In the ISO15693/ISO18000-3 mode 1 RF mode, the M24LR64E-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data is demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). When connected to an antenna, the operating power is derived from the RF energy and no external power supply is required. The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data is generated by the M24LR64E-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data is transferred from the M24LR64E-R at 6.6 Kbit/s in low data rate mode and 26 Kbit/s high data rate mode. The M24LR64E-R supports the 53 Kbit/s fast mode in high data rate mode using one subcarrier frequency at 423 kHz.

The M24LR64E-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

The M24LR64E-R provides an Energy-harvesting mode on the analog output pin Vout. When the Energy harvesting mode is activated, the M24LR64E-R can output the excess energy coming from the RF field on the Vout analog pin. In case the RF field strength is insufficient or when Energy harvesting mode is disabled, the analog output pin Vout goes into high-Z state and Energy harvesting mode is automatically stopped.

The M24LR64E-R features a user configurable digital out pin RF WIP/BUSY that can be used to drive a micro controller interrupt input pin (available only when the M24LR64E-R is correctly powered on the V_{CC} pin).

When configured in the RF write in progress mode (RF WIP mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF internal write operation. When configured in the RF busy mode (RF BUSY mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF command progress.

The RF WIP/BUSY pin is an open drain output and must be connected to a pull-up resistor.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24LR64E	CMOSF8H	ST Rousset 8”	CDIP8	Engi assy (1)
M24LR16E (2)	CMOSF8H	ST Rousset 8”	CDIP8	Engi assy (1)

1. CDIP8 is a ceramic package used only for die-oriented reliability trials.
2. M24LR64E is derived from M24LR16E by metal mask option (same silicon process technology, same design core). Qualification data obtained on M24LR16E are applicable to M24LR64E.

The product vehicle used for package qualifications are presented in *Table 4*.

Table 4. Product vehicle used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24LR16E (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
				Subcon Amkor P1
			TSSOP8	ST Shenzhen
				Subcon Amkor P1
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba
				Subcon Amkor P3

1. M24LR64E is derived from M24LR16E by metal mask option (same silicon process technology, same design core). Qualification data obtained on M24LR16E are applicable to M24LR64E.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description									
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size				
						M24LR16E (2)			M24LR64E	
						Lot1	Lot2	Lot3	Lot4	Lot5 (3)
EDR	High temperature operating life after endurance									
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80	-	-
	Data retention after endurance									
	AEC-Q100-005	1million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-	-
LTOL	Low temperature operating life									
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80	-	-
HTSL	High temperature storage life									
	JESD22-A103	Retention bake at 200 °C	80	3	1008 hrs	0/80	0/80	0/80	-	-
WEB	Program/erase endurance cycling + bake									
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 million cycles / 48 hrs	0/80 (4)	0/80 (4)	0/80 (4)	-	-
ESD HBM	Electrostatic discharge (human body model)									
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1500 V	Pass 1000 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 4000 V	Pass 4000 V	Pass 3500 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)									
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)									
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR64E is derived from M24LR16E by metal mask option (same silicon process technology, same design core). Qualification data obtained on M24LR16E are applicable to M24LR64E.
3. Reliability results obtained on lot 5 (refer to PCN MMS-MMY/13/7707).
4. First rejects after 5 million cycles.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24LR16E (2)			M24LR64E
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/1145	0/345	0/1145	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
ELFR (3)	Early failure life rate								
	AEC-Q100-008	HTOL 150 °C, 6V	800	2	48 hrs	0/800	-	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR64E is derived from M24LR16E by metal mask option (same silicon process technology, same design core). Qualification data obtained on M24LR16E are applicable to M24LR64E.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24LR16E(2)			M24LR64E
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	3	N/A	0/1145	0/1145	0/1145	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
ELFR (3)	Early failure life rate								
	AEC-Q100-008	HTOL 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR64E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable to M24LR64E.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24LR16E (2)			M24LR64E
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR64E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable to M24LR64E.
3. THB-, TC-, TMSK-, AC-, and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Apr-2012	1	Initial release.
19-Jun-2012	2	List of qualified commercial products updated in *Table 1*. Added reference to UFDFPN8 (MLP8) 2 x 3 mm package in *Table 2*. *Table 8* updated with latest results.
11-Feb-2013	3	*Table 5* updated with reliability results obtained on lot 5 (refer to PCN MMS-MMY/13/7707).

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QRMMY1127
Qualification report

New product / M24LR04E-R
using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24LR04E-RMN6T/2 M24LR04E-RDW6T/2 M24LR04E-RMC6T/2
Product description	4-Kbit EEPROM with password protection, dual interface & energy harvesting: 400 kHz I^2C bus & ISO 15693 RF protocol at 13.56 MHz
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France

Table 2. Package description

Package description	Qualified assembly plant location	Qualified final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product M24LR04E-R using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The voltage and the external RF carrier frequency covered by this document are:

- I^2C interface:
  - Single supply voltage: 1.8 to 5.5 V
- Contactless interface:
  - ISO 15693 and ISO 18000-3 mode 1 compatible
  - RF carrier frequency: 13.56 MHz ± 7 kHz

The temperature range covered by this document is:

- –40 to 85 °C

The CMOSF8H is a new advanced silicon process technology that has already been qualified in the ST Rousset 8” fab, and is in production for EEPROM products and also for dual interface EEPROM M24LR64/M24LR16E products. This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

1.2 Conclusion

The new product M24LR04E-R using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

The M24LR04E-R device is a dual-interface, electrically erasable programmable memory (EEPROM). It features an I^2C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR04E-R is organized as 512 × 8 bits in the I^2C mode and as 128 × 32 bits in RF mode.

The M24LR04E-R also features an energy harvesting analog output, as well as a user configurable digital output pin toggling during either RF write in progress or RF busy mode.

I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In the ISO15693/ISO18000-3 mode 1 RF mode, the M24LR04E-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). When connected to an antenna, the operating power is derived from the RF energy and no external power supply is required. The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data are generated by the M24LR04E-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the M24LR04E-R at 6.6 Kbit/s in low data rate mode and 26 Kbit/s high data rate mode. The M24LR04E-R supports the 53 Kbit/s fast mode in high data rate mode using one subcarrier frequency at 423 kHz.

The M24LR04E-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

The M24LR04E-R provides an Energy-harvesting mode on the analog output pin Vout. When the Energy harvesting mode is activated, the M24LR04E-R can output the excess energy coming from the RF field on the Vout analog pin. In case the RF field strength is insufficient or when Energy harvesting mode is disabled, the analog output pin Vout goes into high-Z state and Energy harvesting mode is automatically stopped.

The M24LR04E-R features a user configurable digital out pin RF WIP/BUSY that can be used to drive a micro controller interrupt input pin (available only when the M24LR04E-R is correctly powered on the V_{cc} pin).

When configured in the RF write in progress mode (RF WIP mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF internal write operation. When configured in the RF busy mode (RF BUSY mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF command progress.

The RF WIP/BUSY pin is an open drain output and must be connected to a pull-up resistor.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24LR04E	CMOSF8H	ST Rousset 8”	CDIP8	Engi assy (1)
M24LR16E (2)	CMOSF8H	ST Rousset 8”	CDIP8	Engi assy (1)

1. CDIP8 is a ceramic package used only for die-oriented reliability trials.
2. M24LR04E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable.

The product vehicle used for package qualifications are presented in *Table 4*.

Table 4. Product vehicle used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24LR16E (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
				Subcon Amkor P1
			TSSOP8	ST Shenzhen
				Subcon Amkor P1
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba
				Subcon Amkor P3

1. M24LR04E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description									
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size				
						M24LR16E (2)			M24LR04E	
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5 (3)
EDR	High temperature operating life after endurance									
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80	-	-
	Data retention after endurance									
	AEC-Q100-005	1million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-	-
LTOL	Low temperature operating life									
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80	-	-
HTSL	High temperature storage life									
	JESD22-A103	Retention bake at 200 °C	80	3	1008 hrs	0/80	0/80	0/80	-	-
WEB	Program/erase endurance cycling + bake									
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 million cycles / 48 hrs	0/80 (4)	0/80 (4)	0/80 (4)	-	-
ESD HBM	Electrostatic discharge (human body model)									
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1500 V	Pass 1000 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 4000 V	Pass 4000 V	Pass 4000 V	Pass 3500 V
ESD MM	Electrostatic discharge (machine model)									
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)									
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR04E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable.
3. Reliability results obtained on lot 5 (refer to PCN MMS-MMY/13/7707).
4. First rejects after 5 million cycles.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24LR16E (2)			M24LR04E
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/1145	0/345	0/1145	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
ELFR (3)	Early failure life rate								
	AEC-Q100-008	HTOL 150 °C, 6V	800	2	48 hrs	0/800	-	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR04E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24LR16E(2)			M24LR04E
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	3	N/A	0/1145	0/1145	0/1145	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
ELFR (3)	Early failure life rate								
	AEC-Q100-008	HTOL 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR04E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24LR16E (2)			M24LR04E
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80	-
					504 hrs	0/80	0/80	0/80	
					1008 hrs	0/80	0/80	0/80	
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. M24LR04E is derived from M24LR16E by metal mask option (same silicon process technology, same design core. Qualification data obtained on M24LR16E are applicable.
3. THB-, TC-, TMSK-, AC-, and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
06-Feb-2012	1	Initial release.
02-Apr-2012	2	*Table 8* updated with ESD CDM results.
11-Feb-2013	3	*Table 5* updated with reliability results obtained on lot 5 (refer to PCN MMS-MMY/13/7707).

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QRMMY1016
Qualification report

New product / M24LR16E-R
using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24LR16E-RMN6T/2 M24LR16E-RDW6T/2 M24LR16E-RMC6T/2
Product description	16 Kbit EEPROM with password protection, dual interface & energy harvesting: 400 kHz I^2C bus & ISO 15693 RF protocol at 13.56 MHz
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France

Table 2. Package description

Package description	Qualified assembly plant location	Qualified final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product M24LR16E-R using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The voltage and the external RF carrier frequency covered by this document are:

- I^2C interface:
  - Single supply voltage: 1.8 to 5.5 V
- Contactless interface:
  - ISO 15693 and ISO 18000-3 mode 1 compatible
  - RF carrier frequency: 13.56 MHz ± 7 kHz

The temperature range covered by this document is:

- –40 to 85 °C

The CMOSF8H is a new advanced silicon process technology that has already been qualified in the ST Rousset 8” fab, and is in production for EEPROM products and also for dual interface EEPROM M24LR64 product. This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

1.2 Conclusion

The new product M24LR16E-R using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The M24LR16E-R device is a dual-interface, electrically erasable programmable memory (EEPROM). It features an I^2C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR16E-R is organized as 2048 × 8 bits in I^2C mode and as 512 × 32 bits in ISO 15693 and ISO 18000-3 mode 1 RF mode.

The M24LR16E-R also features an energy harvesting analog output, as well as a user configurable digital output pin toggling during either RF write in progress or RF busy mode.

I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In ISO15693/ISO18000-3 mode 1 RF mode, the M24LR16E-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). When connected to an antenna, the operating power is derived from the RF energy and no external power supply is required. The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data are generated by the M24LR16E-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the M24LR16E-R at 6.6 Kbit/s in low data rate mode and 26 Kbit/s high data rate mode. The M24LR16E-R supports the 53 Kbit/s fast mode in high data rate mode using one subcarrier frequency at 423 kHz.

The M24LR16E-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

The M24LR16E-R provides an energy harvesting mode on the analog output pin Vout. When energy harvesting mode is activated, the M24LR16E-R can output the excess energy coming from the RF field on the Vout analog pin. In case the RF field strength is insufficient or when energy harvesting mode is disabled, the analog output pin Vout goes into high-Z state and energy harvesting mode is automatically stopped.

The M24LR16E-R features a user configurable digital out pin RF WIP/BUSY that can be used to drive a microcontroller interrupt input pin (available only when the M24LR16E-R is correctly powered on the V_{CC} pin).

When configured in RF write in progress mode (RF WIP mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF internal write operation. When configured in RF busy mode (RF BUSY mode), the RF WIP/BUSY pin is driven low for the entire duration of the RF command progress, from the RF command Start Of Frame (SOF) until the end of the command execution.

The RF WIP/BUSY pin is an open drain output and must be connected to a pull-up resistor.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24LR16E-R	CMOSF8H	ST Rousset 8”	CDIP8	Engi assy (1)

1. CDIP8 is a ceramic package used only for die-oriented reliability trials.

The product vehicle used for package qualifications is presented in *Table 4*.

Table 4. Product vehicle used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24LR16E-R	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
				Subcon Amkor P1
			TSSOP8	ST Shenzhen
				Subcon Amkor P1
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba
				Subcon Amkor P3

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24LR16E-R			
						Lot 1	Lot 2	Lot 3	Lot 4 (2)
EDR	High temperature operating life after endurance								
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80	-
	Data retention after endurance								
	AEC-Q100-005	1million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
LTOL	Low temperature operating life								
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80	-
HTSL	High temperature storage life								
	JESD22-A103	Retention bake at 200 °C	80	3	1008 hrs	0/80	0/80	0/80	
WEB	Program/erase endurance cycling + bake								
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 million cycles / 48 hrs	0/80 (3)	0/80 (3)	0/80 (3)	-
ESD HBM	Electrostatic discharge (human body model)								
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1500 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 4000 V	Pass 4000 V	Pass 3500 V
ESD MM	Electrostatic discharge (machine model)								
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)								
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Reliability results obtained on lot 4 (refer to PCN MMS-MMY/13/7707).
3. First rejects after 5 million cycles.

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Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M24LR16E-R		
						Lot1	Lot2	Lot3
PC	Preconditioning: moisture sensitivity level 1							
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/1145	0/345	0/1145
THB (2)	Temperature humidity bias							
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80
TC (2)	Temperature cycling							
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80
TMSK (2)	Thermal shocks							
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25
AC (2)	Autoclave (pressure pot)							
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80
HTSL (2)	High temperature storage life							
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80
ELFR (2)	Early failure life rate							
	AEC-Q100-008	HTOL 150 °C, 6V	800	2	48 hrs	0/800	-	0/800
ESD CDM	Electrostatic discharge (charge device model)							
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-

1. See *Table 9: List of terms* for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M24LR16E-R		
						Lot1	Lot2	Lot3
PC	Preconditioning: moisture sensitivity level 1							
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	3	N/A	0/1145	0/1145	0/1145
THB (2)	Temperature humidity bias							
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80
TC (2)	Temperature cycling							
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80
TMSK (2)	Thermal shocks							
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25
AC (2)	Autoclave (pressure pot)							
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80
HTSL (2)	High temperature storage life							
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80
ELFR (2)	Early failure life rate							
	AEC-Q100-008	HTOL 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)							
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-

1. See *Table 9: List of terms* for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) (1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M24LR16E-R		
						Lot1	Lot2	Lot3
PC	Preconditioning: moisture sensitivity level 1							
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345
THB (2)	Temperature humidity bias							
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80
TC (2)	Temperature cycling							
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80
TMSK (2)	Thermal shocks							
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25
AC (2)	Autoclave (pressure pot)							
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80
HTSL (2)	High temperature storage life							
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	168 hrs	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80
ESD CDM	Electrostatic discharge (charge device model)							
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-

1. See *Table 9: List of terms* for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC-, and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
18-Oct-2011	1	Initial release.
18-Jan-2012	2	List of qualified commercial products updated in *Table 1*. Added *Table 8*. *Table 6* updated with latest results.
07-Feb-2013	3	*Table 5* updated with reliability results obtained on lot 4 (refer to PCN MMS-MMY/13/7707).

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Appendix D: Errata sheet (rev. 2):

M24LR04E-R, M24LR16E-R, M24LR64E-R Errata sheet

M24LR04E-R, M24LR16E-R and M24LR64E-R device limitations

Silicon identification

This errata sheet applies to STMicroelectronics M24LR04E-R, M24LR16E-R and M24L64E-R dual interface EEPROM products. The devices will be referred to M24LRxxE-R throughout the document.

The full list of part numbers is shown in *Table 1*. These parts can be identified physically by their marking or directly on the application by reading the product revision byte in I^2C.

Identification by marking

Table 1. Device summary

Reference	Package	Ordering code	Internal sales type	First line marking	
				Revision 0xF	Revision 0xE and below
M24LR04E-R	TSSOP08	M24LR04E-RDW6T/2	M24LR04RDW6T2UTE	404EU	4BEUB
	MLP	M24LR04E-RMC6T/2	M24LR04RMC6T2UGE	404E	4BEB
	SO8N	M24LR04E-RMN6T/2	M24LR04RMN6T2UGE	24L04ER	24LBERB
	Bare die	M24LR04E-RUW20/2	M24LR04ERUW20/U2	N/A	N/A
M24LR16E-R	TSSOP08	M24LR16E-RDW6T/2	M24LR16RDW6T2UTE	416EU	4DEUB
	MLP	M24LR16E-RMC6T/2	M24LR16RMC6T2UGE	416E	4DEB
	SO8N	M24LR16E-RMN6T/2	M24LR16RMN6T2UGE	24L16ER	24LDERB
	Bare die	M24LR16E-RUW20/2	M24LR16ERUW20/U2	N/A	N/A
M24LR64E-R	TSSOP08	M24LR64E-RDW6T/2	M24LR64EDW6T2UTA	464EU	4FEUB
	MLP	M24LR64E-RMC6T/2	M24LR64EMC6T2UGA	464E	4FEB
	SO8N	M24LR64E-RMN6T/2	M24LR64EMN6T2UGA	24L64ER	24LFERB

Identification by I^2C read

The part can be identified by reading in I^2C the product revision byte included in the system area.

The product revision is the Most Significant Nibble of the byte located at address 0x911 in the system area (Device select code E2 = 1).

All the limitations described in this document have been fixed for product revision 0xE and below.

1 Product evolution

The following table gives a summary of the fix status.

Legend for *Table 2*: A = workaround available, grayed = fixed.

Table 2. Product evolution summary

Limitation	Rev F	Rev E and below
Section 2.1: RF field drop during I^2C write cycle execution	A	
Section 2.2: SetRstEHEn command not functional in Addressed mode	A	

2 Limitations

2.1 RF field drop during I^2C write cycle execution

Description

The M24LRxxE-R can be powered though an external V_{CC} pin or via an induced voltage generated by the RF field.

Occasionally, an RF field drop occurring during an I^2C write cycle might have an impact on the M24LRxxE-R internal supply voltage. This drop can be caused either by an amplitude modulation of the RF field or a by a significant current spike on the Energy Harvesting pin (V_{OUT}). It might result in the I^2C bus to be blocked or in an incomplete programming cycle.

Workaround

- Revision 0xF

  It is recommended to avoid any RF activity during the execution of I^2C write operations.

  When this not possible, please follow the recommendations below to improve your design robustness:

  – After an I^2C write operation, it is recommended to check that the data programmed have been correctly updated and reprogram them if necessary.

  – When the M24LRxxE-R I^2C bus is blocked (no acknowledge), the I^2C master shall power-on/power-off the chip (V_{CC} pin) to regain control of the M24LRxxE-R. An optimized method to do this is to power the M24LRxx-R V_{CC} pin using a microcontroller I/O.

- Revision 0xE and below

  This limitation has been corrected by a design fix that avoids blocking the I^2C interface. T_Prog flag (b7 of the control register located at address 920h in system area) indicates the correct duration of the write cycle. Refer to the product datasheets for details.

2.2 SetRstEHEn command not functional in Addressed mode

Description

When the *SetRstEHEn* command is sent in Addressed mode, all M24LRxxE-R devices execute the command whatever their unique identifier (UID).

Consequently, it is not possible to address an M24LRxxE-R device individually to set or reset the Energy Harvesting.

This limitation does not prevent designers from using the Energy Harvesting command but this command must be executed in a Non-addressed mode or in Select mode.

- When the command is used in Non-addressed mode, all M24LRxxE-R devices in reader operating volume will execute the command.
- When the command is executed in Select mode, only the M24LRxxE-R previously put in select state will execute the *SetRstEHEn* command.

Workaround

- Revision 0xF

  Set and reset the Energy harvesting using only Non-addressed or Select mode.

- Revision 0xE and below

  This limitation has been corrected by a design fix that allows supporting the full SetRstEHEn command features. Refer to the product datasheets for details.

3 Revision history

Table 3. Document revision history

Date	Revision	Changes
23-Apr-2012	1	Initial release.
11-Feb-2013	2	Added silicon revisions 0xE and below and updated limitation descriptions accordingly.

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Document Revision History

Date	Rev.	Description of the Revision
February 04, 2013	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

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